HyFiSS: A Hybrid Fidelity Stall-Aware Simulator for GPGPUs

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***Abstract*—The widespread adoption of GPUs has driven the development of GPU simulators, which, in turn, lead advancements in both GPU architectures and software optimization. Trace-driven cycle-accurate Cycle-accurate simulators, which provide detailed microarchitectural models and clock-level precision, come at the cost of extended simulation times and require high computational resources. Their scalability has become a bottleneck. A growing trend is the adoption of cycle-approximate simulators, which introduce mathematical modeling of partial hardware units and utilize sampling to accelerate simulation. However, this approach faces challenges regarding the accuracy of performance predictions.**

To address these limitations, we introduce HyFiSS, a hybrid fidelity stall-aware GPU simulator. HyFiSS features fine-grained stall events tracking and attribution by constructing a detailed execution pipeline model for various stall events on *Streaming Multiprocessors* (SMs). It accurately emulates the thread block scheduler behavior using real-time scheduling logs and utilizes sampling based on thread block sets to minimize the precision loss due to fine-grained sampling points on the microarchitectural state. We achieve a balance between reliability, speed, and the level of simulation detail, especially regarding bottlenecks. By evaluating a diverse set of benchmarks, HyFiSS achieves a mean absolute percentage error in predicting active cycles that is comparable to the state-of-the-art cycle-accurate simulator Accel-Sim. Moreover, HyFiSS achieves a substantial 12.8× speedup in the simulation efficiency compared to Accel-Sim. HyFiSS also requires at least 3.2× less disk storage than both Accel-Sim and another state-of-the-art cycle-approximate simulator PPT-GPU due to its efficient *SASS* (*Streaming Assembler*) traces compression. With precise, per-cycle stall events statistics, HyFiSS can provide accurate GPU performance metrics and stall cause reporting. This significantly simplifies performance analysis, bottleneck identification, and performance optimization tasks for researchers, making it easier to enhance GPU performance effectively.

***Index Terms*—GPGPU Simulation, Workload Characterization**

I. Introduction

Graphics Processing Units (GPUs) are extensively used in compute-hungry domains, such as high-performance computing and artificial intelligence. To optimize GPU hardware or software running on it [1]–[5], GPU simulators played a key role in understanding the execution details and identifying performance bottlenecks. Various industrial and academic GPU simulators [6]–[13] have been meticulously designed, encompassing the associated performance analysis models [14]–[24]. These simulation frameworks[1] typically allow users to describe GPU architectures with high-level parameters, and provide a performance model for the specified architecture to guide system optimizations.

Despite the advancements in GPU simulation frameworks, achieving a comprehensive balance between simulation fidelity and speed remains challenging for the existing open-source GPU simulation frameworks [9]. A cycle-accurate simulation demands to emulate the behavior of all components in the GPU architecture and their interactions in each cycle. It usually incurs significant overheads, which usually grows exponentially with the size or complexity of the simulated workload. Such overheads could lead to substantial time costs for iterative simulations in system optimizations [21], [25], [26]. Meanwhile, researchers often need rapid, iterative performance feedback. The slow speed of cycle-accurate simulators can hardly meet these needs [22], [27], [28].

A growing trend is the adoption of cycle-approximate simulators, which simulate compute instructions and memory instructions separately [8], [29]–[31]. They utilize mathematical modeling and multi-level sampling strategies to improve simulation speed by orders of magnitude. Unlike comprehensive, high-fidelity cycle-accurate simulations, cycle-approximate approaches abstract local details through mathematical modeling. These models include the roofline model [14], [15], parallelism based on latency hiding [16], [17], interval-based analysis [29]–[31], and compilation-based analysis of data or control flow graphs [18], [21]–[23]. However, these models often lack a robust methodology for accurately representing complex hardware states. Consequently, they may overlook established prior knowledge such as well-documented hardware features or parameters familiar to hardware architects and software optimization researchers. In particular, they do not adequately account for the impact of hardware stalls on

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[1]In this paper, we refer to GPU simulators and performance analysis models collectively as simulation frameworks.

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performance, which has an important impact on the application execution on GPUs. As a result, cycle-approximate simulators may encounter limitations in achieving precise performance evaluation and detailed bottleneck analysis [21].

To overcome these drawbacks, we introduce HyFiSS, a cycle-approximate, hybrid fidelity stall-aware simulator. Figure 1 illustrates our design principles, which begin with identifying typical stall events through abstract analysis from real hardware ❶. We then choose different fidelities of hardware pipelines to construct the simulator ❷. Via simulation and stall event attribution of sampled real application traces, HyFiSS provides stall event stacks ❸, which are similar to CPI stacks in CPUs that indicate the distribution of execution time for instructions [32]–[35]. The abstracted stall events are further refined based on this feedback, thereby influencing the design of HyFiSS ❹. Once the stall events are established and stabilized, HyFiSS can identify hardware bottlenecks through attribution analysis, enabling optimization of the hardware design ❺. Figure 2 quantitatively compares the prediction performance of two state-of-the-art simulators—Accel-Sim [6], [7] (a cycle-accurate simulator, denoted as *ASIM*), and PPT-GPU [8] (a cycle-approximate simulator, denoted as *PPT*)[2]—and HyFiSS across a suite of 35 applications consisting of 1,784 kernels. These are compared against performance metrics obtained from a real NVIDIA QUADRO GV100 GPU (hereafter referred to as the GV100 GPU, denoted as *NCU*) using *Nsight Compute* [36].

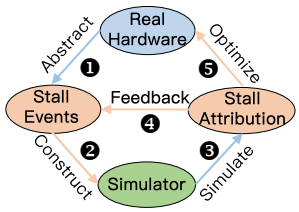


Fig. 1: Conceptual Overview of Our Design Principles.

As shown in Figure 2a Accel-Sim's simulation of a program is up to ten million times slower than real execution on GPU, resulting in significant cumulative delays during the iterative simulation to evaluate numerous design strategies [37]. Conversely, PPT-GPU offers markedly faster simulations—up to three orders of magnitude faster than Accel-Sim—attributable to a reuse distance analysis model and a parallelized compute model with lower fidelity. However, PPT-GPU suffers from larger prediction errors in performance metrics. Figure 2b-Figure 2c exhibit that PPT-GPU's mean absolute percentage errors (MAPEs) in active cycles, instructions per cycle (hereafter referred to as IPC) and occupancy reach 255.8%, 72.0%, and 27.39%, respectively. In contrast, the detailed microarchitectural modeling of Accel-Sim results in much lower errors of only 21.9%, 33.3%, and 3.62%.

Whereas, HyFiSS makes up for the gap between them in terms of simulation speed and prediction accuracy. HyFiSS demonstrates the MAPE of only 39.9% in predicting active cycles, outperforming PPT-GPU. It achieves an average 12.8× speedup over Accel-Sim. Further experimental results show that HyFiSS offers an average 3.2× reduction in trace disk storage compared to both Accel-Sim and PPT-GPU. Furthermore, HyFiSS demonstrates remarkable accuracy in predicting critical cache performance metrics. The mean absolute error (MAE) for the L1 and L2 cache hit rates, and occupancy is only 5.68%, 13.53%, and 10.26%, respectively. Furthermore, HyFiSS offers comprehensive bottleneck analysis for programs running on NVIDIA GPUs, which gives hardware designers and software programmers valuable feedback to optimize the hardware or program due to its stall-aware feature.

The contributions of this paper are listed as follows:

- We analyzed stall events closely linked to hardware constraints and focuses on the primary stall types impacting pipeline execution. This inspired us to develop a hybrid fidelity simulation. It incorporates various levels of fidelity—from highly detailed to highly abstracted—to forge an effective and simulation-efficient abstraction of the entire GPU hardware.
- Our approach enables hybrid-fidelity stall events tracking and accurately attributes a stall cycle to its root cause. We have introduced an attribution algorithm, which builds the foundation for detailed analysis of performance bottlenecks and effective workload characterization.
- We propose a Streaming Multiprocessors sampling algorithm based on *Cooperative Thread Array-Sets*. This algorithm relies on *SASS* (*Streaming Assembler*) traces to rectify the inaccuracies introduced by fine-grained sampling, such as simulating only one warp or thread block, which often diminishes the resource contention in execution pipelines. Our sampling not only improves the simulation accuracy but also significantly enhances the efficiency.
- We have open-sourced our stall-aware GPU simulator [38], HyFiSS. It is a clock-driven simulator for pipeline execution with a parallelized cache hierarchy model based on reuse distance analysis. Besides the simulator, we also provide a set of tools for *SASS* traces extraction, sampling, statistical analysis, etc. The encouraging experimental results suggest the effectiveness of our approach.

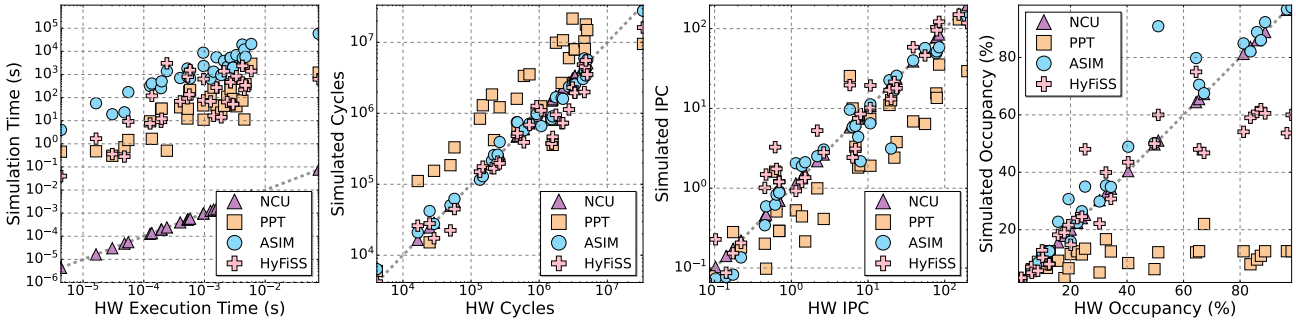
II. Background & Motivation

This section provides the necessary theoretical background to understand our design principles and motivations.

A. GPU Hardware Architecture

We briefly introduce the NVIDIA GPU architecture organization using the example of the GV100 GPU [6], [7], [39]–[41], as illustrated in Figure 3. NVIDIA GPUs consist of an array of *Streaming Multiprocessors* (SMs) that execute in parallel. Each SM contains a variety of scalar and vector ALU units, as well as specialized cores like Tensor Cores [1]. Each SM includes a private L1 cache, which also serves as shared memory. All SMs access a unified L2 cache through a high-bandwidth interconnect network.

[2]We select PPT-GPU as the baseline because it is—to our knowledge—the only open-source and executable cycle-approximate GPU simulator.



(a) Simulation Time. (b) Active Cycles (c) Instructions Per Cycle. (d) Achieved Occupancy.

Fig. 2: Prediction Performance Comparison of Accel-Sim [7] and PPT-GPU [8].

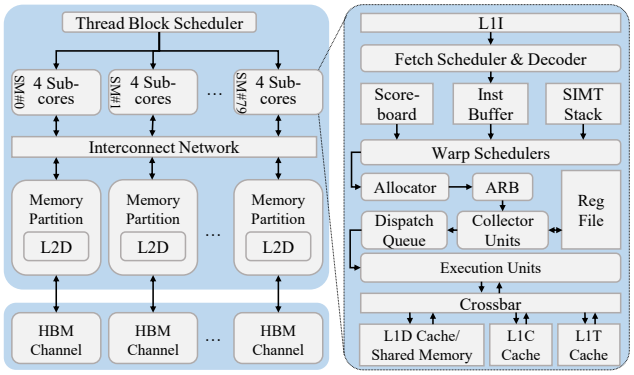


Fig. 3: Architecture Organization of the GV100 GPU.

B. Parallel Execution Pattern of CUDA Programs

To effectively simulate the programs on GPUs, it is crucial to understand both the complexity of GPU hardware and the multilayered parallel execution patterns employed by programs. In the CUDA programming model, users define the grids and thread blocks (aka *Cooperative Thread Arrays*, hereafter referred to as CTAs) organization and the distribution of computational tasks across available threads [42]. The device code written by users is compiled into kernels, which execute concurrently on the SMs following the *Single Instruction, Multiple Threads* (SIMT) paradigm. Threads within each CTA are grouped into warps, which constitute the basic scheduling unit. At its core, the simulators simulate the complex multi-level parallelism of CTAs on multi-SMs, capturing both the simultaneous execution across SMs and the concurrent warp processing within pipelines, with warps as the fundamental granularity of simulation.

The execution of threads is managed by a multi-tiered hardware scheduler. The scheduling of instructions execution on GPUs is conducted at two levels: the warp schedulers dispatch warps to time-multiplexed execution units [43]–[48], whereas the CTA scheduler allocates CTAs to execute on SMs [49]–[51]. Typical simulation frameworks for GPGPUs adopt a Round-Robin (hereafter referred to as *RR*) strategy for CTA scheduling, which sequentially allocates consecutive CTAs to different SMs when there are sufficient resources available [6]–[8], [49], [50]. However, our observations of the CTA scheduler behavior on a real GV100 GPU reveal deviations from the *RR* strategy.

We build our tracing tool on top of NVIDIA's *NVBit* dynamic binary instrumentation tool [52] to collect the runtime CTA scheduler behavior on a real GV100 GPU. Figure 4 illustrates the normalized distribution of CTAs and warp instructions across different SMs for 9 applications from widely-used benchmark suites including Rodinia [53] and PolyBench [54]. The *SM IDs* have been sorted based on the distribution of CTAs. A general observation suggests that the distributions of CTAs and warp instructions for all the applications exhibit varying degrees of imbalance. Figure 5 presents a time-view of CTA scheduling behavior for the *b+tree* application. It displays the IDs of the CTAs allocated to the first four SMs, based on information traced from the CTA scheduler. This reveals a non-sequential and non-uniform pattern of CTA allocation during runtime. The actual hardware likely maintains a schedulable queue influenced by the on-the-fly information, resulting in a non-uniform CTA distribution across SMs.

C. Stalls in Execution

Stall refers to the phenomenon where the GPU pipeline experiences a pause during execution and is not able to continue executing. GPUs aim at hiding pipeline latency with *Thread-Level Parallelism* (TLP) and *Instruction-Level Parallelism* (ILP), while stalls create pipeline bubbles, detrimentally affecting the execution efficiency [55]. Stalls not only directly lead to pipeline resource wastage and performance loss but also amplify performance bottlenecks through their cascading effects, significantly reducing the performance of the entire system. Morpheus [56] reported the performance degradation in K-means clustering applications due to stalls from the reduced L2 cache hit rates. These cache misses cause a cascading effect, stalling the pipeline and preventing the issue of subsequent instructions, leaving most SMs to be idle. Consequently, the performance with 68 SMs barely exceeds that with 10 SMs and is 50% less than with 20

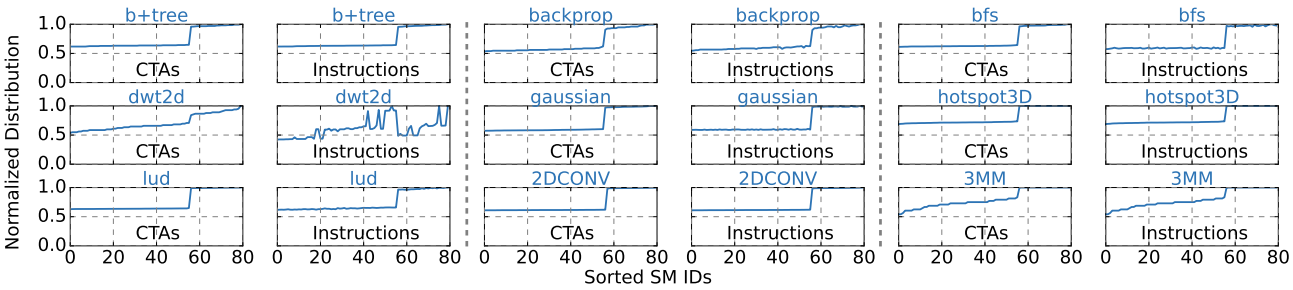


Fig. 4: Normalized Distribution of CTAs and Warp Instructions on SMs.

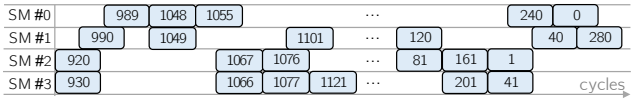


Fig. 5: Time-View of CTA Scheduling Across SMs for *b+tree*.

SMs, highlighting the amplified systemic effects of stalls. Thus, stalls are the key issue in GPU's performance bottleneck analysis [14]–[17], [21], [22], [29]–[31], [46], [57]–[60].

Generally, the stalls are categorized into seven types:

- **Memory Structural Stall** (*MemStruct*) is caused by the resource contention within the memory subsystem.
- **Memory Data Stall** (*MemData*) arises from latency in data access and data dependencies among operands for memory instructions.
- **Compute Structural Stall** (*ComStruct*) arises from resources contention within GPU compute units.
- **Compute Data Stall** (*ComData*) results from data dependencies among operands for compute instructions.
- **Synchronization Stall** (*Sync*) arises from thread synchronization and inter-thread communication.
- **Control Stall** (*Ctrl*) occurs when branch divergence invalidates the instructions queued in the instruction buffer.
- **Idle Stall** (*Idle*) happens in the absence of active warps ready for instruction issue.

Motivation. The hardware complexity of GPUs is not only high but also continually increasing as their architectures evolve to support advancements in performance and features. For example, the GV100 GPU contains 80 SMs and 5,120 CUDA cores, while later generations of GPUs, such as Tesla A100 and Hopper H100 GPUs have greater numbers of SMs and CUDA cores. In addition, GPU hardware architecture involves a hierarchical mapping and scheduling process, along with elaborate interactions between various execution units. Numerous concurrently executing threads, each maintaining independent execution contexts, require synchronization and communication among them. These intertwining factors pose significant challenges to simulation accuracy and speed. We believe that the ideal simulator should achieve a comprehensive balance between reliability, speed, and bottleneck analysis capability; this is the goal of our work. Designing a GPU simulator from the perspective of stalls might be an effective approach not only for revealing performance bottlenecks but also for enabling potential optimization opportunities in the simulation of GPU systems, improving both accuracy and speed. The following section III and section IV will discuss our design principles and implementation.

III. Design Principles and Key Algorithms

This section outlines the design principles of HyFiSS, a simulation employing hybrid fidelity built on multiple levels of abstraction. Our design principles relies on two key algorithms. One is stall attribution, which tracks stall events and attributes them to a stall cycle. The other is SM sampling based on *Cooperative Thread Array-Sets*, which makes it sufficient to simulate one SM instead of all SMs.

A. Simulation with Hybrid Fidelity

Simulation frameworks inevitably involve accepting a certain level of inaccuracy, and fidelity grading is essential for faster simulation [9]. We thoroughly analyze the root causes of all stall events for GPU hardware. Based on this analysis, we present a hybrid fidelity simulation design that integrates various levels of hardware fidelity, thus enabling an effective abstraction of the entire hardware system.

Figure 6 illustrates our simulator design, featuring a single SM pipeline with key multi-SM shared components like L2 cache and HBM. The GPU execution pipeline contains a variety of units, each serving a specific function. The detailed explanations of these units are as follows:

- *SP* stands for Single-Precision Floating Point Units;
- *DP* denotes Double-Precision Units;
- *SFU* is the Special Function Units;
- *INT* refers to the Integer-Precision Units;
- *TC* stands for Tensor Cores;
- *LDST* represents the Memory Pipeline;
- *CU* is identified as the Collector Units;
- *ARB* refers to the arbitrator selecting non-conflicting accesses for the register files.

For each unit, we use three fidelity levels: high, medium, and low fidelities to simulate the GPU execution pipeline. High-fidelity modules simulate every hardware state for maximum precision. Medium fidelity, in contrast, relies on latency models that approximate hardware behavior, sacrificing some accuracy for efficiency. Low-fidelity simulation uses empirical

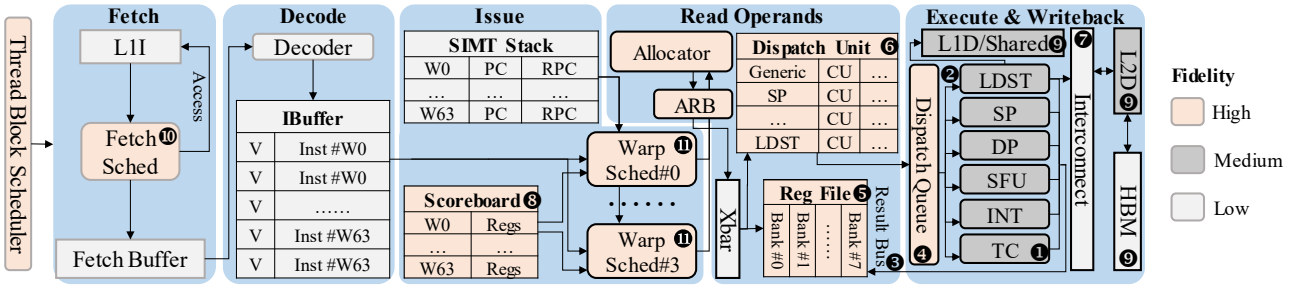


Fig. 6: The Illustration of GPU Execution Pipeline with Hybrid Fidelity.

latency models, providing a rough estimation and occasionally omitting certain hardware states for simplicity. Table I lists the key stall events, such as data dependency, resource contention, synchronization of warp instructions, etc., all of which are explicitly associated with the hardware units. As shown in Figure 6 and Table I, most hardware units related to stall events are designed to be at least medium fidelity.

Key components directly related to stalls, such as the fetch scheduler, scoreboard, warp schedulers, operand collectors, and register files, are simulated with high fidelity, as depicted in Figure 6. Execution units like *SP Unit*, *INT Unit*, and *DP Unit* are modeled with medium fidelity, encapsulating their execution with latency models that simulate instruction delays. For the memory hierarchy, including L1 and L2 caches, we employ medium-fidelity simulations based on the established *Reuse Distance* model. Reuse distance, reflecting the lifespan of cache blocks, provides a quantitative estimation of the cache hits rates in a sequence of memory references [8], [47], [61]–[68]. To ensure a realistic simulation, we use full *Streaming Multiprocessor* (full-SM) memory access sequences to estimate the shared L2 cache's hit rates, with a detailed explanation provided in subsection IV-E.

We simulate the interconnect network and HBM in low fidelity due to their inherent complexity and the relative infrequency of interconnect network congestion as a stall event [9]. Accurate simulation of the interconnect network can typically be achieved using latency and bandwidth models. For HBM accessed by global memory requests, we adopt an estimated *Average Memory Access Time* (*AMAT*) [69], [70], which will be detailed in subsection IV-E.

B. Stall Events Tracking and Attribution

Our simulator provides a detailed tracking of stall events that occur in the GPU execution pipeline. To systematically investigate the impact of stalls on GPU performance, it is essential to establish the connections between stalls and their underlying causes. Since different stall events can occur simultaneously and may belong to various stall types, identifying the primary root stall type can be challenging.

For instance, bank conflicts in the write-back stage in an earlier cycle can cause execution units to remain occupied as they need to retry the write-back in subsequent cycles, thereby delaying subsequent instruction issues. The direct factor for this stall was the execution pipeline saturation; however, the underlying indirect root cause can be traced back to bank conflicts from the preceding cycle. Similarly, high-latency memory accesses might not stall the instruction issue immediately but can prevent it in a later cycle. These indirect stall events, therefore, are a result of accumulated delays from various saturation points or contention in the system, ending in a stall cycle. We hereby formally define the following terms:

- *stall cycle*, a cycle in which at least one warp scheduler is unable to issue an instruction from its issue queue. In an ideal case, each warp scheduler would reach its peak issue rate without any stalls.
- *root stall type*, the type of the initial or the primary event responsible for triggering subsequent stalls in the pipeline.
- *direct stall events*, the stall events that immediately prevent instructions from being issued.
- *indirect cascade-triggering stall events*, the indirect stall events that trigger additional stall events in later cycles, induced by interactions at different pipeline units.

The goal of our stall attribution algorithm is to accurately pinpoint the *root stall type* for each *stall cycle* by analyzing both the two stall events (as previously defined) across the *stall cycle* and several of its prior cycles.

The identification of *direct stall events* is prioritized as follows: **(1)** The instruction buffer (*IBuffer*) has no active warps available for the current warp scheduler ⑩, directly preventing instructions issue. **(2)** Synchronization ⑪, data dependencies ⑧, or unsatisfied execution unit issuing mutual exclusion ❷ may prevent the issuing of queued instructions. The stall event ❷ means that it is prohibited to issue two consecutive instructions to the same execution unit to weaken contention and improve overall instruction throughput. **(3)** A shortage of free operand collectors (*CUs*) ❻ likely prevents the instruction from obtaining necessary operands, blocking its progression in the pipeline.

Stall events triggered by pipeline stages after *CUs* in an earlier cycle will exacerbate the release blockage of the *CUs* at the current *stall cycle*. Considering the time cost of the algorithm, we designate a set of four consecutive cycles $\langle cycle\#0,\ cycle\#1,\ cycle\#2,\ stall\ cycle\rangle$ for backtracking to identify *indirect cascade-triggering stall events*. The prioritization sequence is as follows: **(1)** Bank conflicts ❺ at *cycle #2*

TABLE I: Stall Events, Their Occurrence Units, and Types.

Stall Events and Occurrence Units	Stall Type
Execution Unit Pipeline Saturation ❶* Execution Unit Issuing Mutual Exclusion ❷ Result Bus Saturation ❸ Dispatch Queue Saturation ❹ Bank Conflict ❺ No Free Operands Collector Units ❻	MemStruct ComStruct
Interconnect Network Congestion ❼	MemStruct
Data Dependence in Scoreboard ❽	MemData/ComData
Cache/Global Memory Access ❾	MemData
No Active Warps ❿	Idle
Barrier synchronization ⓫	Sync

* Numerical labels mark event numbers and occurrence units in Figure 6.

result in the *CUs* remaining occupied during the current *stall cycle*. **(2)** Execution unit pipeline saturation ❶ or the dispatch queue saturation ❹ at *cycle #2*. **(3)** High-latency memory accesses ❾, result bus saturation during the writeback ❸, and interconnect network congestion ❼ at *cycle #1*. Given that most optimized applications efficiently mitigate congestion in the interconnect network [9], and the result bus saturation is a direct consequence of bank conflicts at *cycle #0* (which has been factored into our analysis during the stall attribution of *cycle #1*). Therefore, we identify high-latency memory accesses, typically occurring in the *LDST Unit*, as the primary contributors to the current *stall cycle*.

algorithm 1 prioritizes *direct stall events* as the probable root cause of a *stall cycle*. However, if there are underlying *indirect cascade-triggering stall events* potentially driving these direct events, it will be investigated further to determine the root cause. Additionally, when multiple *direct stall events* or *indirect cascade-triggering stall events* occur, we determine the root cause of the *stall cycle* based on the extent to which the events affect the instructions issue.

It is crucial to note that the stall events listed in Table I were not abstracted in a single step during the construction of the simulator. Initially, only a subset of the events in Table I was constructed at the early design stage. Through the process of stall events tracking and attribution, we observed that some *stall cycles* could not be attributed to one of the initially defined stall events. This finding prompted an expansion of the stall event abstractions based on the current observed *stall cycles*. Therefore, Table I presents the finalized set of stall events after the stabilization of the iterative *Feedback* process depicted in Figure 1. This iterative approach can be extended to the construction of simulators for other hardware platforms, and we will demonstrate the comprehensiveness of the finalized set of stall events in subsection VI-A.

C. SM Sampling Based on CTA-Sets

A widely adopted technique to accelerate architectural simulation is to sample the *phases* of a workload that exhibit repeatable patterns (e.g., IPC) across intervals [27], [37], [71]. We seek to determine which SM has the longest predicted execution time by analyzing the non-stalled execution of its *CTA-Set*—the collection of all CTAs belonging to that SM.

Algorithm 1: Stall Attribution for Warp Schedulers.

Input: Warp scheduler *$sched*, a set of consecutive cycles ⟨*cycle#1*, *cycle#2*, *stall cycle*⟩.
Output: *Root Stall Type* of the current *Stall Cycle*.

```
// Lines 2-13 represent stall events at stall cycle.
if $sched issue an instruction then
    return No Stall;
else if No Active Warps ❿ then
    return Idle Stall;
else if meet conditions ❷❽⓫ then
    if Barrier Synchronization ⓫ then
        return Sync Stall;
    else if Data Dependence in Scoreboard ❽ then
        return MemData/ComData Stall;
    else if Issuing Mutual Exclusion ❷ then
        return MemStruct/ComStruct Stall;
else if No Free Operands Collector Units ❻ then
    // Lines 15-18 represent stall events at cycle#2.
    if Bank Conflict ❺ then
        return MemStruct/ComStruct Stall;
    else if Execution Unit Pipeline Saturation ❶ or
            Dispatch Queue Saturation ❹ then
        // Lines 20-24 represent stall events at cycle#1.
        if Cache/Global Memory Access ❾ then
            return MemData Stall;
        else if Interconnect Network Congestion❼ then
            return MemStruct Stall;
        else if Result Bus Saturation ❸ then
            return MemStruct/ComStruct Stall;
// Attribution Failure: Stall events have not been abstracted.
return Other Stall;
```

This significantly reduces the time cost by eliminating the necessity of simulating every SM.

GPU workload sampling commonly employs different granularity, such as warp, basic block, or thread block [37], [71], [72]. However, these methods can not accurately evaluate performance stalls caused by resource contention within SMs, for the following reasons:

- Instructions executed before the sampled section alter the microarchitectural state, particularly the caches. This significantly impacts program performance. Simulators must perform a warming-up process before simulating the sampled section. This presents a major challenge [73].
- Sampling at a finer granularity, like basic block or warp, might miss the inherent resource contention due to the decreased number of concurrent instructions [27], [71], [72].
- Without structural information generated during compilation, *SASS* instructions extracted via binary instrumentation struggle to accurately rebuild Control-Flow-Graphs (CFGs) for basic block sampling.

To address these limitations, we propose SM sampling with the granularity of thread block sets (*CTA-Sets*). The offline sampling process runs concurrently with the actual GPU execution when extracting traces, ensuring that the time overhead for sampling is negligible. Unlike other methods [37] that use

clustering to assess the similarity among basic blocks, warps, or CTAs, we select the SM anticipated to have the maximal execution duration as the sampling point for simulation. These *CTA-Sets* with longer non-stall execution time, when execution units are fully utilized with a saturated issue rate, tend to consume more cycles in a resource-constrained SM pipeline. We predict the maximal anticipated execution duration of the *CTA-Set* on each SM by their non-stall execution time.

Let the set of execution units categories be U_{eu}, with the i-th category of execution unit eu^i (such as an *SP unit*) having a count of N^i_{eu} and an individual instruction execution latency of Lat^i_{eu}. Furthermore, let the number of instructions extracted from an SM be NI^i_{sm}, if these instructions can be dispatched to eu^i. Then, disregarding the issue rate of instructions, the execution time of eu^i can be calculated as:

$$C^i_{NonStall} = \frac{NI^i_{sm}}{N^i_{eu}} + (Lat^i_{eu} - 1). \tag{1}$$

And the total execution time $C_{NonStall}$ for all instructions can be calculated as $\max_{i \in U_{eu}} C^i_{NonStall}$, disregarding the instruction issue rate. Assume that *IRate* denotes the saturated issue rate of all warp schedulers within an SM, representing the maximum number of instructions that can be issued per cycle by a single SM. Next, we consider the total execution time $C^{FullIR}_{NonStall}$ with warp schedulers operating at full issue rate. Therefore, $C^{FullIR}_{NonStall}$ can be calculated as:

$$C^{FullIR}_{NonStall} = \max_{i \in U_{eu}} \frac{C^i_{NonStall} \times N^i_{eu}}{\min(N^i_{eu}, IRate)}. \tag{2}$$

We calculate $C^{FullIR}_{NonStall}$ for each *CTA-Sets* and select the SM with the maximum execution time as the sampling point to be fed into our execution pipeline model for simulation.

IV. HyFiSS Simulator Implementation

This section describes the implementation of HyFiSS simulator. HyFiSS utilizes MPI for process-based parallelism and employs a hybrid-fidelity execution pipeline model with simulation gating for balancing fully event-driven and cycle-driven simulation. It is highly parameterized, enabling users to model various generations of NVIDIA GPUs by simulating *SASS* traces. We set configurable parameters derived from publicly available documentation [39], [40], [42] and a micro-benchmark suite from Accel-Sim [74].

A. Overview of HyFiSS

Figure 7 shows the HyFiSS architecture, which consists of (1) A *Tracing Tool*, built on top of *NVBit* [52], which records application configurations, processes SM sampling based on CTA-Sets, compresses *SASS* instructions, and captures the real CTA scheduler behavior. (2) A suite of *Parsers* interprets application configurations, the traced real CTA scheduler behavior, and user-defined hardware parameters. (3) A fast *Unpacker* decodes warp instructions for the *Execution Pipeline* and *Reuse Distance* model. (4) A *Reuse Distance* model predicts L1 and L2 cache hit rates. (5) A hybrid fidelity and stall-aware *Execution Pipeline* model tracks the stall events

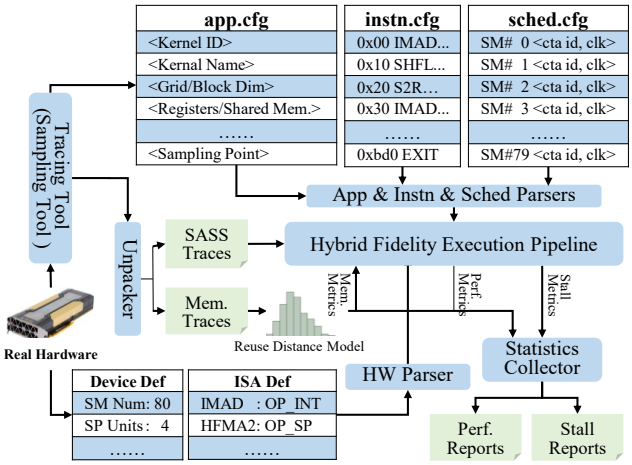


Fig. 7: Architecture of HyFiSS Simulator.

and performs the stall event attribution, and (6) A *Statistics Collector* provides a detailed simulation summary. We then provide more detailed descriptions of the key components, highlighting their roles and interplay within HyFiSS.

B. Tracing Tool

Our *Tracing Tool*, built on top of *NVBit* APIs [52], captures runtime information with minimal performance interference.

1) Application Configurations: The *Tracing Tool* generates an application configuration (*app.cfg*) that includes kernel details, as shown in Figure 7. This information guides the initialization of all warp instances with the grid and block dimensions and manages the concurrency of CTAs. Additionally, it reports the sampling points—the SM ID used during subsequent simulation—as outlined in subsection IV-C, exemplified by the last entry in *app.cfg*.

2) Traces Compression: Traces compression featured in the *Tracing Tool* reduces the size of traces extracted from real GPUs. Although the instructions executed by different warps within a kernel may vary in order, they share identical *program counters* (PCs) and instruction sequences. Compared to Accel-Sim [7] and PPT-GPU [8], HyFiSS significantly reduces traces storage requirements by retaining unique $\langle pc, mask \rangle$ pairs for instructions within each warp. It stores the instruction strings including opcodes, operands, and memory addresses in *instn.config*. This enables efficient restoration of instruction strings during unpacking by querying *instn.config*.

3) CTA Scheduling Information: HyFiSS accurately captures the dynamic CTA scheduler behavior on real GPUs with an integrated monitor in the *Tracing Tool*. This monitor logs each CTA's issue with SM IDs and timestamps into *sched.cfg*. HyFiSS then reproduces CTA scheduling and execution from *sched.cfg*, mirroring the real hardware behavior.

C. Sampling Tool

Our *Sampling Tool*, integrated within the *Tracing Tool*, collects the count of instructions dispatched to various execution units within each CTA. To avoid the computational

TABLE II: Benchmarks Evaluated for 35 Applications Across 7 Suites, Comprising 1,784 Kernels.

	Applications (#kernels)	Traces Size (ASIM, PPT, HyFiSS)	Simulation Time	Applications (#kernels)	Traces Size (ASIM, PPT, HyFiSS)	Simulation Time	Domain
[53]	*backprop* (2)	311M, 200M, 75M	3m, 2s, 7s	nw (255)	577M, 374M, 241M	11m, 2m, 3m	ML/Bioinformatics
	b+tree (2)	783M, 884M, 183M	7m, 2s, 27s	*dwt2d* (10)	299M, 246M, 77M	5m, 33s, 17s	Data Structure/DSP
	hotspot (1)	161M, 24M, 41M	57s, 1s, 3s	*hotspot3D* (100)	11G, 23G, 4.7G	6h, 2m, 36m	Physics Simulation
	gaussian (300)	32G, 8.5G, 2.1G	65m, 44s, 23m	lud (300)	27G, 11G, 4.6G	2h, 42s, 14m	Linear Algebra
	huffman (46)	1.5G, 283M, 351M	12m, 38s, 2m	nn (1)	2.0M, 3.3M, 1.1M	4s, 1s, 1s	Data Compress./Mining
	bfs (24)	2.1G, 1.4G, 1.5G	39m, 11s, 7m	*pathfinder* (5)	738M, 217M, 161M	5m, 9s, 11s	Graph Algorithms
	cfd (10)	679M, 9G, 220M	9m, 33s, 21s	lavaMD (1)	20G, 648M, 4.5G	3h, 11s, 50s	Physics Simulation
[54]	*2DConv* (1)	1.1G, 2.6G, 233M	23m, 1s, 30m	*3DConv* (99)	1.3G, 3.6G, 795M	13m, 33s, 15m	Image Processing
	3mm (3)	3.3G, 18G, 2.5G	92m, 46s, 4m	*gemm* (1)	1.3G, 6G, 898M	30m, 12s, 1m	Linear Algebra
	atax (2)	264M, 2G, 212M	33m, 26s, 47s	*gesummv* (1)	350M, 3G, 283M	35m, 2m, 2m	Linear Algebra
	bicg (2)	264M, 2G, 212M	32m, 1m, 48s	*gramschm* (3)	79M, 506M, 62M	16m, 22s, 18m	Linear Algebra
	mvt (2)	264M, 2G, 212M	32m, 1m, 48s				Linear Algebra
[75]	gemm_train (8)	11G, 6.1G, 2.1G	2h, 6m, 9m	gemm_inf (8)	11G, 6.2G, 2.1G	2h, 7m, 9m	CNN
	rnn_inf (133)	25G, 33G, 11G	2h, 6m, 7m	rnn_train (291)	40G, 40G, 14G	88m, 91m, 8m	RNN
	conv_inf (11)	1.5G, 1.3G, 448M	22m, 4m, 28s				CNN
[76]	AlexNet (22)	32G, 30G, 12G	6h, 48m, 16m	SqueezeNet (30)	29G, 44G, 12G	16h, 20m, 11m	CNN
	GRU (2)	676K, 2.4M, 428K	19s, 1s, 3s	*LSTM* (1)	296K, 1.1M, 208K	23s, 1s, 2s	RNN
[77]	GemmEx (1)	9.3G, 3.2G, 2.2G	3h, 45s, 1m				Linear Algebra
[78] [79]	LULESH (81)	857M, 611M, 273M	20m, 3m, 4m	PENNANT (25)	4.8G, 3.6G, 1.1G	11m, 4m, 19m	Mesh Hydrodynamics

complexity of clustering methods, we leverage user-defined hardware parameters, such as the number of execution units and instruction execution latency, to predict the execution time of an SM and select the candidate to simulate. The offline sampling strategy effectively distributes the sampling overhead across the runtime of each real GPU thread, making it virtually imperceptible.

D. Traces Unpacking & Parsing

A fast *Unpacker* is developed to convert the instructions from the compressed format to HyFiSS's execution format. It retrieves and parses the instructions from the compressed file (*kernel.sass*) based on the unique identifier $\langle kernel\_id, pc \rangle$ defined in *instn.config*, where additional metadata such as instruction types, operand types, and operands are also recorded. Then, the *Trace-Parser* categorizes instructions and directs them using $\langle kernel\_id, pc, global\_warp\_id \rangle$ to the simulator for subsequent simulation.

E. Reuse Distance Model

We utilize multiprocessing to simulate the hit rates of L1 and L2 caches for global memory access across each SM, leveraging memory instructions. The calculation of the *Average Memory Access Time* (*AMAT*) of HyFiSS is similar to that of other simulators [8]. To accurately simulate the queuing overhead within the interconnect network, we regulate the instruction throughput rate of the latency model for *LDST Unit*. This ensures that it does not exceed the maximum bandwidth capacity of the interconnect network. In addition, the latency of global memory accesses reflects the queuing overhead for off-chip memory.

V. Evaluation

A. Experimental Setup

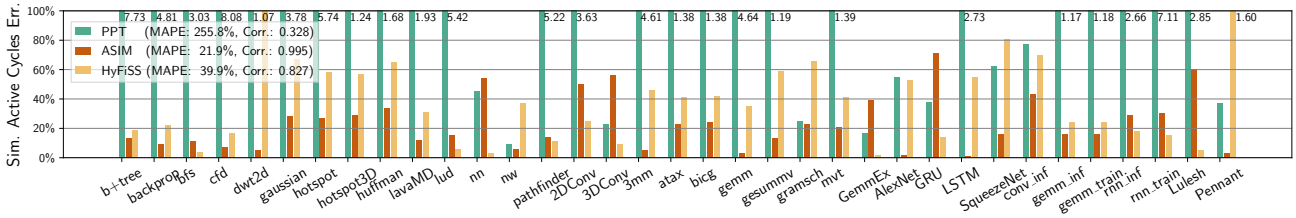
Our experimental system is equipped with two 32-core Intel® Xeon® processors with hyper-threading capability.

TABLE III: NVIDIA QUADRO GV100 GPU Configurations.

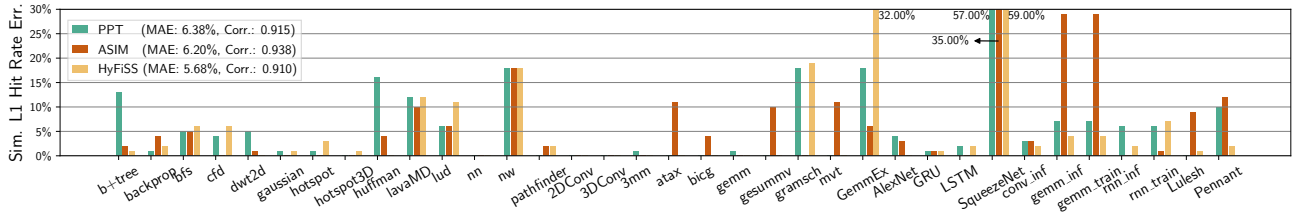
Parameter	Value
Number of SMs	80
Warp Schedulers per SM	4 Two-Level [80], [81] Round-Robin Schedulers
Max Warps, Threads, CTAs per SM	64 / 2048 / 32
Core Clock Frequency	1447 MHz
Shared Memory Size per SM	Configurable up to 96 KB
L1 Data Cache	32 KB, 4 sets, 32B line, 4 Banks, LRU
L2 Data Cache	6 MB, 24 Sets, 64B line, 64 Banks, LRU
Registers per SM	65536, 8 Banks

We use the hardware configuration of the widely-modeled NVIDIA QUADRO GV100 GPU [39]. Its simulation parameters are listed in Table III. We compare HyFiSS to the state-of-the-art cycle-accurate simulator Accel-Sim [7] and cycle-approximate simulator PPT-GPU [8], all simulating *SASS* instructions. Both Accel-Sim and PPT-GPU use *NVBit* APIs [52] to extract *SASS* instructions, a feature that HyFiSS also possesses while providing further capabilities. As mentioned earlier, HyFiSS supports CTA scheduler behavior extraction, traces compression, and sampling based on *CTA-Sets*. Performance metrics measured on a real GV100 GPU using NVIDIA's *Nsight Compute* [36] serve as the baseline.

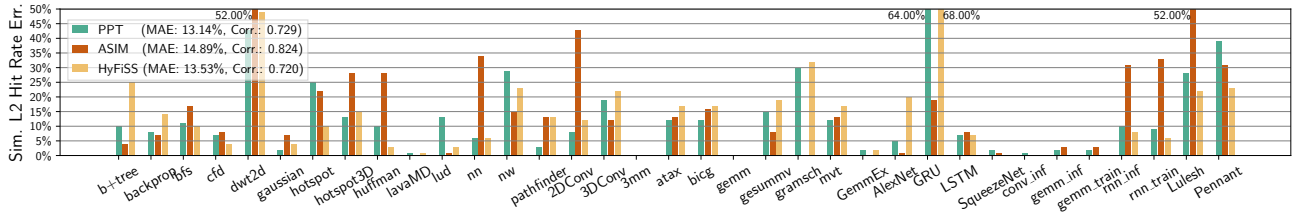
Table II lists the benchmark applications from various domains used for validation. We run 35 applications with a total of 1,784 kernels. These applications are from the *cuBLAS* library [77], the heterogeneous computing benchmark suite PolyBench [54], Rodinia [53], the fluid dynamics benchmark LULESH [78], [82], the deep learning basic operators benchmark suite DeepBench [75], the DNN benchmark suite Tango [76] and the unstructured mesh mini-app benchmark PENNANT [79]. The convolutional layer training program from DeepBench [75] and the CifarNet model from Tango [76]



(a) Simulated Active Cycles Error Rate (MAPE).



(b) Simulated L1 Cache Hit Rate Error Rate (MAE).



(c) Simulated L2 Cache Hit Rate Error Rate (MAE).

Fig. 8: Prediction Performance Comparison of Active Cycles and Cache Hit Rates.

are omitted because their traces are too large, making simulation time unacceptable for Accel-Sim. All workloads are compiled using CUDA 11.0 with the compute capability *sm70* for the Volta architecture.

B. Prediction Accuracy

We use the mean absolute error (MAE) to evaluate the prediction accuracy of percentage metrics, and the mean absolute percentage error (MAPE) for that of non-percentage metrics. We use Pearson's correlation coefficient (Corr.) to show the correlation between the predicted and measured metrics. Figure 8 and Table IV illustrates the prediction performance of Accel-Sim, PPT-GPU, and HyFiSS for active cycles and cache hit rate, compared to the real hardware results.

The error rates for active cycle predictions are detailed in Figure 8a. Note that we sum up the active cycles across all simulated kernels as the total active cycles for that application. Accel-Sim shows the best performance in predicting active cycles, with the lowest MAPE of 21.9% and a prediction correlation near 1. HyFiSS, benefiting from a detailed stall analysis-based compute model, achieves the MAPE of 39.9% and a prediction correlation of 0.827. This performance significantly surpasses that of PPT-GPU, which has a MAPE of 255.8% and a correlation coefficient of 0.328 (refer to Figure 2b for an application-specific comparison).

Predictions of L1 and L2 cache hit rates are compared in Figure 8b and Figure 8c respectively. For each application, the hit rate is calculated as the sum of hit requests divided by the total requests for all simulated kernels. HyFiSS achieves the lowest MAE of 5.68% in predicting the L1 cache hit rate, slightly outperforming Accel-Sim (6.20% MAE) and PPT-GPU (6.38% MAE). All simulators exhibit prediction correlations above 0.910 for L1 cache hit rate. For L2 cache hit rate, HyFiSS has an MAE of 13.53%, slightly higher than PPT-GPU's 13.14% but lower than Accel-Sim's 14.89%.

TABLE IV: Error Rate and Corr. Comparison of Metrics.

(MAPE, Corr.)	**Accel-Sim**	**PPT-GPU**	**HyFiSS**
Active Cycles	21.9%, 0.995	255.8%, 0.328	39.9%, 0.827
GMEM Requests	269.4%, 0.173	88.0%, 0.999	82.8%, 0.998
IPC	33.3%, 0.901	72.0%, 0.711	65.5%, 0.928
(MAE, Corr.)	**Accel-Sim**	**PPT-GPU**	**HyFiSS**
L1 Hit Rate	6.20%, 0.938	6.38%, 0.915	5.68%, 0.910
L2 Hit Rate	14.89%, 0.824	13.14%, 0.729	13.53%, 0.720
Occupancy	3.62%, 0.974	27.39%, 0.416	10.26%, 0.910

* GMEM Requests: Global Memory Requests.

Table IV also illustrates the prediction performance for other metrics besides active cycles, L1, and L2 hit rates. Global memory (GMEM) requests predictions are best anticipated by HyFiSS with a 82.8% MAPE and 0.998 correlation, outperforming PPT-GPU's MAPE and closely following its high correlation. Accel-SIM's MAPE is significantly higher at 269.4%, indicating HyFiSS's superiority in predicting global memory requests. For each application, we calculate the av-

erage achieved occupancy across all kernels as the program's achieved occupancy. HyFiSS's 10.26% MAE is better than PPT-GPU's and only second to Accel-Sim, which leads with a 3.62% MAE. HyFiSS also holds a strong second with a 0.910 correlation, trailing behind Accel-Sim's 0.974 but notably ahead of PPT-GPU's 0.416 (see Figure 2d for an application-specific comparison). The IPC prediction comparisons in Table IV reveal that Accel-Sim leads in accuracy and correlation, while HyFiSS performs well but with room for improvement (see Figure 2c). IPC is a comprehensive metric influenced by numerous factors, such as HyFiSS's inaccurate estimation of the total number of instructions in non-sampled *CTA-Sets*.

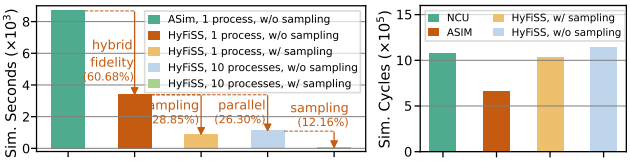
Overall, the prediction accuracy of HyFiSS closely aligns with the results achieved by Accel-Sim.

C. Simulation Time & Traces Disk Storage

TABLE V: Simulation Time & Traces Disk Storage.

	Simulation Time	Traces Disk Storage
Accel-Sim	2d 2h 21m 35s	269.7 GB
PPT-GPU	3h 24m 20s	263.4 GB
HyFiSS	3h 55m 12s	81.3 GB

Table V compares the simulation time and traces disk storage of Accel-Sim, PPT-GPU, and HyFiSS across all benchmarks. HyFiSS achieves a 12.8× speedup compared to Accel-Sim, due to its hybrid-fidelity strategy that reduces simulation overhead unrelated to stalls tracking. However, it is 15.1% slower than PPT-GPU, because PPT-GPU utilizes optimized parallel discrete event simulation (PDES) [83] and process-based parallelization [84]. In contrast, HyFiSS only employs a simple MPI framework for multiprocessing acceleration. Besides speedups, HyFiSS also exhibits a high trace compression ratio, consuming 3.3× and 3.2× less disk storage than Accel-Sim and PPT-GPU, respectively. It means that HyFiSS can support the simulation with larger trace sizes.



(a) Simulation Speedup. (b) Accuracy Loss.

Fig. 9: Ablation Study to Quantify HyFiSS Benefits.

To understand the benefits of hybrid fidelity, SM sampling based on *CTA-Sets*, and process-based parallelism employed by HyFiSS, Figure 9a compares the simulation times of Accel-Sim and HyFiSS using a *cuBLAS* [77] matrix multiplication program ($M, K, N = 2048$). Compared to Accel-Sim's serial simulation, hybrid fidelity alone reduces HyFiSS simulation time by 60.68%. Independently applying SM sampling and 10-process parallel simulation further reduce HyFiSS simulation time by 28.85% and 26.30%, respectively. By integrating all these techniques, HyFiSS achieves a 116× speedup over Accel-Sim with only minor accuracy loss as Figure 9b shows.

D. Irregular Applications and Alternative Microarchitectures

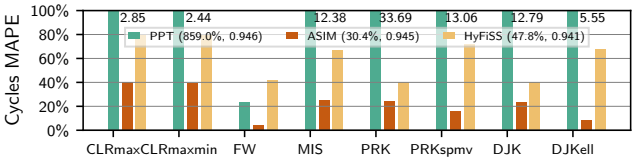


Fig. 10: Prediction Performance Comparison for Pannotia.

To demonstrate HyFiSS's applicability in predicting the accuracy of irregular applications, we compare its accuracy against Accel-Sim and PPT-GPU using the Pannotia benchmark suite [85]–[87] with the GV100 configuration. As shown in Figure 10, HyFiSS demonstrates competitive accuracy against Accel-Sim and significantly surpasses PPT-GPU.

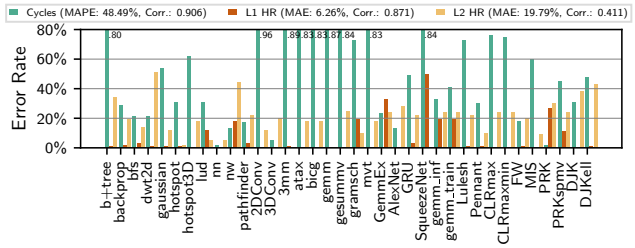


Fig. 11: Prediction Performance on the Ampere A100 GPU.

We then modeled the Ampere A100 GPU [88], which is equipped with 108 SMs and features 40 MB of L2 cache along with 192 KB/SM of L1 cache. The predicted accuracy of HyFiSS across all applications, including the Pannotia benchmark suite, is shown in Figure 11. HyFiSS demonstrates a MAPE of 48.49% in predicting simulated cycles, which is less accurate compared to the GV100 GPU simulation. Note that we did not alter the simulator design and only adjusted the hardware and *ISA* configuration based on publicly available documents [88], [89]. This might not fully capture the actual hardware details. Our future work involves calibrating HyFiSS with the A100 GPU. The increased number of SMs in the A100 GPU enhances its simulation efficiency, because the number of CTAs allocated to each sampled SM decreases.

E. SASS vs. PTX Simulation

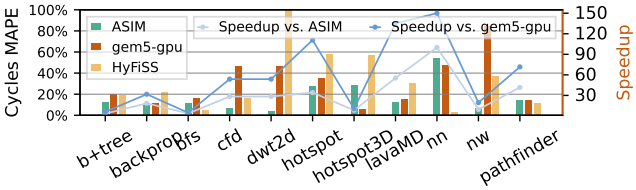


Fig. 12: Prediction Accuracy of *SASS* and *PTX* Simulation.

We compared the prediction performance of HyFiSS and Accel-Sim (*SASS* simulation) against gem5-gpu [10] (*PTX*

simulation) using the Rodinia benchmark suite [53], as illustrated in Figure 12. In most applications, *SASS* simulation achieves higher accuracy than *PTX* simulation, as the latter may oversimplify microarchitectural behaviors [90].

VI. Case Studies

This section details how HyFiSS reveals performance bottlenecks, which is useful for potential system optimization.

A. Stall Distribution

Figure 13a illustrates the distribution across 9 different stall types for various applications. It reveals that only a few applications (*backprop* and *gaussian*) have a *No Stall* percentage exceeding 30%, indicating that most programs experience significant stalls throughout their execution. Nearly all applications are primarily affected by four stall categories: *ComStruct*, *ComData*, *MemStruct*, and *MemData*. Based on their proportions, we classify applications as either *memory-bound* or *compute-bound*, as shown in Table II (*memory-bound* applications are underlined and italicized). Furthermore, *Sync*, *Ctrl* and *Idle* stalls have a minimal impact on all applications.

Our stall attribution methodology enables accounting for almost all *stall cycles* by attributing them to specific stall events, with only a negligible fraction classified as *Others*. This indicates that our defined stall events are comprehensive.

Figure 13b presents the distribution of *ComStruct* and *MemStruct* stall events. *GRU* and *LSTM* did not exhibit these two stall types, hence they are not presented. The data shows that *Execution Unit Pipeline Saturation*, *Dispatch Queue Saturation*, *Bank Conflict*, and *No Free Operand Collector Units* are the primary causes of *ComStruct* and *MemStruct* stalls. The SM experiences the highest percentage of stalls during the operands collection, writeback, and instructions dispatch stages. This insight suggests that architectural design should focus on optimizing these critical stages.

Figure 13c presents the distribution of *MemData* stall events. This reveals that most applications experience few stalls due to *Data Dependencies* and can effectively utilize the cache, resulting in fewer *Global Memory Access* stalls for applications with high cache hit rates. However, applications such as *cfd*, *dwt2d*, *nn*, *nw*, etc., face notable stalls due to their patterns of non-contiguous and random memory access. Optimizing cache utilization remains a key strategy for improving performance across many applications. For those encountering extensive *Global Memory Access* stalls, it is crucial to consider alternative approaches, such as redesigning access patterns, to improve memory bandwidth efficiency and reduce latency.

ComData stall events are all generated by the *Scoreboard*, we will not present a separate distribution for *ComData* stalls.

B. Execution Time and Instructions Distribution Analysis

Figure 14 illustrates the execution time and executed instructions distribution of execution units. This reveals a positive correlation between the execution time of an execution unit and the total number of instructions belonging to it. However, it is crucial to note that the workload of execution units varies among applications due to program characteristics such as data precision and computation patterns. For example, in the *nw* application, *SP Units* are rarely utilized. Therefore, monitoring the workload of execution units is essential for performance optimization. Execution units used by high-frequency instructions should be prioritized for performance tuning and resource scaling to prevent them from becoming bottlenecks and impacting the overall execution efficiency.

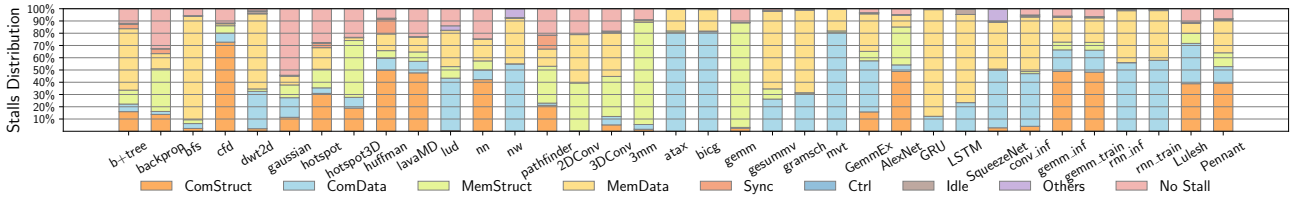
C. Accuracy of Stall Events Distribution

We select and compare three stall metrics from *Nsight* [36] that align with HyFiSS's counting logic: the average latency between two consecutive instructions waiting for scoreboard dependencies, CTA barriers, and available execution units. Figure 15 shows the results using Rodinia [53]. For the vast majority of applications, HyFiSS provides accurate metrics against *Nsight*. The discrepancies arise from inaccurate conflict management entries in HyFiSS to capture certain conflicts, such as scoreboard entries, barrier synchronization monitoring entries, and dispatch queue entries. During periods of rapid drop in conflicts (e.g., scoreboard dependencies of *bfs*), these entries become overly redundant and cause the smaller delays in issuing related instructions. This results in deviations from real hardware in terms of the average latency between two consecutive instructions and subsequently leads to lower average values. However, this situation has minimal impact on capturing most stall events in the pipeline and further, on execution cycle prediction.

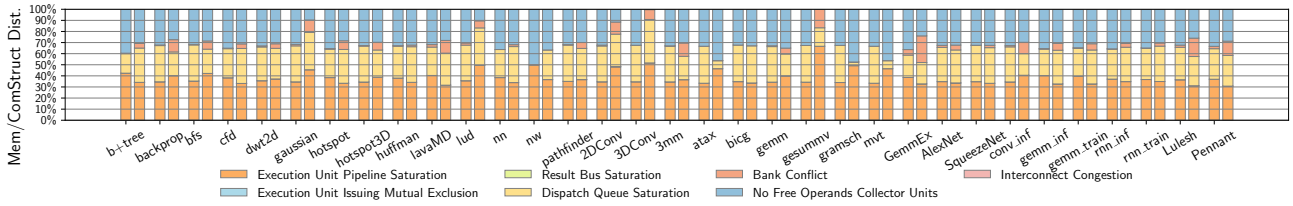
D. Simulation of Concurrent Kernels

In Figure 16, we simulate the concurrent performance of eight *cuBLAS* kernels with the GV100 GPU configuration. Each performs a 1024×1024 matrix multiplication concurrently to achieve a 2048×2048 matrix multiplication. Our simulation shows, concurrency reduces the simulation cycles by 32.87% and increases the occupancy by 14.12%, resulting in a 48.13% IPC increase. Since L1 cache stores data copies from multiple concurrent kernels, its hit rate decreases slightly. Conversely, the L2 cache hit rate improves because it stores a single copy of data reused among concurrent kernels. By comparing the performance of concurrent kernels obtained through *Nsight*'s *Range Replay* mode, HyFiSS shows competitive accuracy.

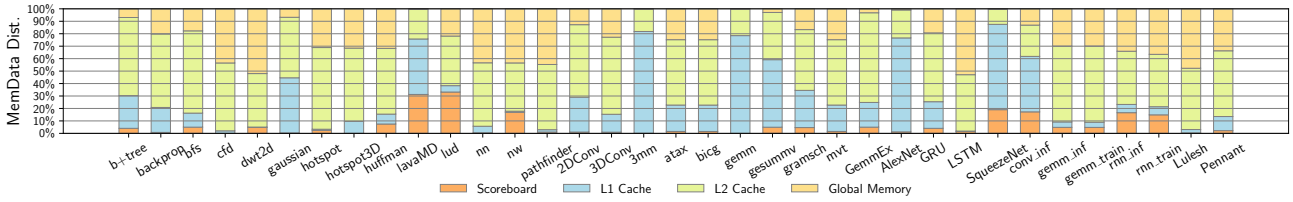
Figure 16f illustrates the stall distribution of concurrent kernels execution. With the increase in the number of concurrent instructions, the proportions of *MemStruct* and *ConStruct* stalls rise. Figure 16g indicates that concurrent instructions further complicate register mapping and significantly increase bank conflicts. Meanwhile, Figure 16h shows that the distribution of *ComStruct* stalls remains relatively stable because the proportion of compute instructions has not changed significantly. Here we primarily present stall events distribution rather than their absolute cycle count, as the former provides more intuitive insights for optimizing concurrent kernel execution.



(a) Stall Distribution Across Different Stall Types for Various Applications.



(b) Distribution of MemStruct (left bar) and ComStruct (right bar) Stall Events.



(c) Distribution of MemData Stall Events.

Fig. 13: Distribution of Stall Types and Stall Events.

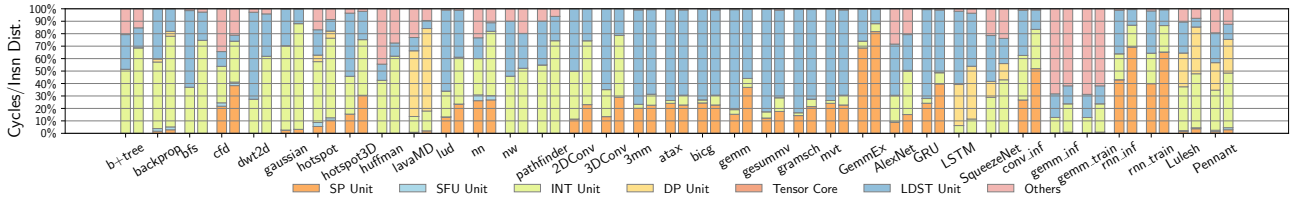
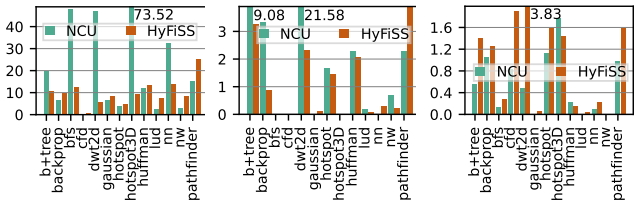
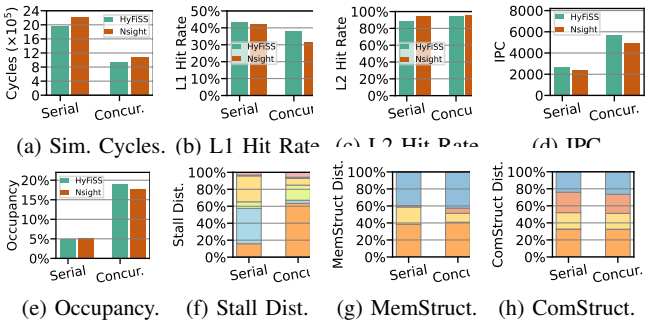


Fig. 14: Execution Time (left bar) and Executed Instructions (right bar) Distribution of Execution Units.



(a) Scoreboard. (b) Barrier. (c) Execution Units.

Fig. 15: Average Latency Between Consecutive Instructions.



(a) Sim. Cycles. (b) L1 Hit Rate (c) L2 Hit Rate (d) IPC

(e) Occupancy. (f) Stall Dist. (g) MemStruct. (h) ComStruct.

Fig. 16: Prediction of Concurrent Kernels on GV100. The legends in Figure 16f through Figure 16h match those in Figure 13.

E. Optimizing Architecture Design with HyFiSS

For a specific architecture and application, HyFiSS captures the root stall events in each cycle and provides the representative stall event stacks. Besides bottleneck detection, they also offer valuable insights to guide architecture design improvement. The fast and precise simulation of HyFiSS enables efficient comparison of different design choices. As a demonstration, Figure 17 shows the effect of changing (a) the number of SMs, (b) the warp scheduling policy from *LRR* to *Greedy-Then-Oldest* [91] (*GTO*), and (c) the L1 cache size with *hotspot*. Instead of enumeration of parameters, architects

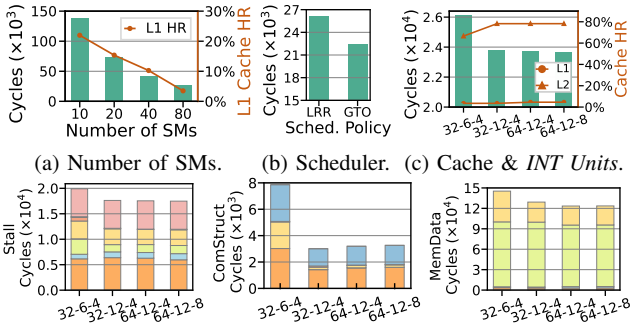
can leverage the stall event stacks to quickly and accurately identify the main bottlenecks and optimization opportunities. Figure 13a identifies the primary stall types of *hotspot*: *ComStruct* and *MemData*. In Figure 17, we try to optimize the architecture to reduce the above two stall types for *hotspot*. For *ComStruct* stalls, we simply increase the number of *INT Units* to mitigate *Execution Unit Pipeline Saturation*, as the high distribution of INT Unit indicated by Figure 14. For *MemData* stalls, Figure 13c highlights that the root stall event is high L2 cache access latency. Our goal is to enhance L1 and L2 cache hit rates to reduce high memory access latencies. L1 cache enlargement shows minimal impact due to *hotspot*'s weak temporal locality, leading us to enlarge the L2 cache size. Figure 17 confirms these optimizations decreased *MemData* stall cycles by 15.45%, cut global memory access latency by 38.16%, and lowered the *Sync* stalls overhead. Furthermore, boosting the number of *INT Units* reduced stall cycles of *Execution Unit Pipeline Saturation* by 47.04%. Collectively, the three steps—doubling the L1 and L2 cache sizes, and the number of INT Units—illustrated in Figure 17c represent the improvements that reduced the execution time of *hotspot* on the GV100 GPU by 9.29%.

VII. Related Work

A. Simulation Frameworks

1) With Tightly-Coupled Hardware Parameters: Simulators with tightly-coupled hardware parameters primarily use clock-driven simulation and heavily depend on detailed hardware parameters, covering general-purpose simulators like GPGPU-Sim [6], Accel-Sim [7], NVArchSim [9], MacSim [12] for Intel GPUs, MGPUSim [11] for AMD GPUs, and the FPGA-based simulator Vortex [92]. Some application-specific simulators, such as Vulkan-Sim [93] with ray-tracing support, [94] with CuDNN and PyTorch support, [1] with Tensor Core units, and graphics rendering simulators like Emerald [95] and ATTILA [96] with OpenGL support, also require detailed hardware parameters. However, such detail-oriented simulators often trade-off simulation speed for accuracy, hindering extensive application analysis. PPT-GPU [8] simplifies the compute model but fails to capture stalls accurately due to lacking detailed microarchitectural modeling.

2) With Loosely-Coupled Hardware Parameters: Advanced simulation models with loosely-coupled hardware parameters, like roofline [14], [15] and interval-based methodologies such as GPUMech [29], GCoM [31], and MDM [30], as well as latency hiding models [16], [17], enable faster performance predictions. However, their less detailed nature can obscure understanding performance bottlenecks. Data and control flow graph-based approaches [18], [21]–[23] attempt to uncover data dependencies but may fail to account for dynamic stalls. Moreover, critical microarchitectural behaviors are often over-simplified in intermediate representations [90], prompting the need for low-level (*SASS*) instruction analysis. Neural network-based models [19], [20] offer quick performance estimates but lack transparency in bottleneck diagnosis.



(a) Number of SMs. (b) Scheduler. (c) Cache & *INT Units*.

(d) Stall Cycles. (e) *ComStruct* Cycles. (f) *MemData* Cycles.

Fig. 17: Performance Effect of GPU Adjustments for *hotspot*. The *x*-axis values in Figure 17c through Figure 17f represent the L1 cache size (KB), L2 cache size (MB), and the number of *INT Units*, respectively. The legends in Figure 17d through Figure 17f match those in Figure 13.

HyFiSS is a simulator with tightly-coupled hardware parameters based on *SASS* instructions, and the first to construct a hybrid-fidelity hardware model based on stall events.

B. Sampling Techniques

For simulation acceleration, *phase*-based sampling of workloads has been extensively researched [97]–[101], utilizing *phase*-detection techniques based on instruction segments similarities [27]. TBPoint [72] extends the *phase*-detection to the kernel and thread block levels. Photon [71] utilizes basic block feature vectors (BBVs) for *phase*-detection and sampling at the kernel, warp, and basic block levels. PKA [25] selects the kernels with the most significant impact on execution time at the kernel level, while Sieve [102] achieves kernel-level sampling using an instruction count-based selection method. Scale-Model [103] employs Sieve [102] for sampling representative kernels and predicting the performance of target GPU system through both scale-modeling and LLC miss rate curves. GT-Pin [37] evaluates the error rates across different sampling granularities. HyFiSS differentiates by performing SM sampling based on *CTA-Sets* to minimize the impact of sampling points on microarchitectural states.

VIII. Conclusion

This work introduces HyFiSS, a cycle-approximate system-level NVIDIA GPU simulator. HyFiSS constructs a hybrid fidelity model according to the correlation between stall events and hardware units. Through tracking and attributing various stall types, HyFiSS can capture their impact during the trace simulation process. Furthermore, the SM sampling and traces compression employed by HyFiSS provide better scalability compared to state-of-the-art simulators. We have open-sourced the complete HyFiSS toolchain. Our results show that HyFiSS achieves a balance between reliability and speed, efficiently supporting bottleneck analysis for various benchmarks.

HyFiSS currently faces a few limitations. It reproduces the dynamic CTA scheduling behavior of real hardware, which

restricts the implementation of user-defined CTA scheduling policies. We plan to support custom CTA scheduling policies in future work. Additionally, further calibration is needed to improve HyFiSS's accuracy, particularly for the Ampere A100 GPU. Based on feedback from *Nsight*, HyFiSS also needs to adjust its conflict management entries. Modern architectures bring significant advancements, such as the *Transformer Engine* in Hopper and uGPUs connected via *NV-HBI* in Blackwell. It is crucial that HyFiSS be extended to support these innovative components. Future improvements will also include adding simulation support for *PTX* instructions to enhance HyFiSS's compatibility with contemporary GPUs.

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ARTIFACT APPENDIX

A. Abstract

This artifact includes the source code of HyFiSS along with the necessary scripts and instructions to reproduce the key experimental results presented in our paper, such as Figure 2, Figure 8, Figure 11, Figure 13, and Figure 14. Additionally, we provide a fully tested docker image with a pre-configured experimental environment for user convenience. To avoid runtime environment issues, we strongly recommend using HyFiSS within our pre-configured docker image.

This artifact also includes necessary scripts to reproduce the results of Accel-Sim, PPT-GPU, and *Nsight Compute*. However, to avoid the need for reproducing the results of these other simulators and tools, and storing their required traces, the results of these tools are provided within our artifact. We have pushed the stable docker image and code of benchmark suites to Zenodo repository [104], and the HyFiSS code along with potentially updatable scripts to GitHub repository [38]. This way, users can easily access and use our artifact while ensuring that it is always up to date.

B. Artifact check-list (meta-information)

- **Compilation:** GCC v7.3 or above, CUDA v11.0 or above, Nsight Compute v2023.1.1 (comes with CUDA v12.0), Make v4.2 or above, Boost C++ Libraries v1.74.0 or above, MPICH v3.3.2.
- **Binary:** NVBit v1.5.1.
- **Run-time environment:** NVIDIA Driver v535.113.01 or above, Python 3.7 or above.
- **Hardware:** Real GV100 and A100 GPUs.
- **Metrics:** *Simulation Time (seconds)*, *Active Cycles*, *IPC*, *Achieved Occupancy*, *Mean Absolute Percentage Error (MAPE)*, *Mean Absolute Error (MAE)*, *Pearson's Correlation Coefficient (Corr.)*, *Distribution of Stall Types and Stall Events*, *Execution Time Distribution of Execution Units*, and *Executed Instructions Distribution of Execution Units*.
- **Output:** Detailed summary Excel files and figures in the paper.
- **Experiments:** Generate experiments using supplied scripts.
- **How much disk space required (approximately)?:** 500 GB.
- **How much time is needed to prepare workflow (approximately)?:** 2 hours. Mostly depends on downloading bandwidth.
- **How much time is needed to complete experiments (approximately)?:** 1 week. Mostly depends on CPU performance.
- **Publicly available?:** Yes.
- **Code licenses (if publicly available)?:** None.
- **Archived (provide DOI)?:** 10.5281/zenodo.13150677

C. Description

1) How to access: GitHub [38] and Zenodo [104].

2) Hardware dependencies: Any Linux system with real GV100 and A100 GPUs and at least 500 GB of free disk space.

3) Software dependencies:

- `libboost_mpi.so >= 1.74.0`
- `git >= 1.8.3.1`
- `gzip >= 1.5`
- `wget >= 1.14`
- `g++ >= 7.3`
- `make >= 4.2`
- `docker >= 19.03`
- `ncu >= 2023.1.1`
- `nvcc >= 11.0`
- `mpirun == 3.3.2`
- `python >= 3.7`
  - `pandas == 1.1.5`
  - `Pillow == 9.5.0`
  - `numpy == 1.21.6`
  - `matplotlib == 3.5.3`
  - `scipy == 1.1.0`
  - `xlrd == 1.1.0`
- `mpiexec == 3.3.2`

4) Data sets or models: None.

D. Installation using our pre-configured docker image

1) Download our pre-configured docker image micro57.tar.gz—the non-root username and password are both *micro57*, and the root password is also *micro57*—from Zenodo repository, save it to the <Download>/ directory, unzip it, and load it:

```
$ wget -O <Download>/micro57.tar.gz https://zenodo.org/records/
  13150677/files/micro57.tar.gz?download=1
$ gzip -d <Download>/micro57.tar.gz
$ docker load -i <Download>/micro57.tar
```

2) Check the <IMAGE_ID> of the loaded docker image, then create a container, and run it:

```
$ docker image list    # check the <IMAGE_ID>
$ docker run --gpus all -it <IMAGE_ID> /bin/bash
```

3) We have already included the files that need to be cloned and downloaded in the docker image, so users only need to check for updates in the corresponding repositories and build them:

```
$ su micro57    # enter the password: micro57
$ source ~/.bashrc
$ cd ~/HyFiSS && git pull && make clean && make all -j
$ cd ~/HyFiSS/tracing-tool && make clean && make
$ cd ~/HyFiSS/sass-split && make clean && make
$ cd ~/Paper-Figures && git pull
$ cd ~/Results-Process-Scripts && git pull
$ cd ~/Self-Simulated-Results && git pull
$ cd ~/simulator-apps && ./cleanall.sh && ./buildall.sh
```

E. Installation from the source code

We strongly recommend that users follow the directory tree structure provided below, including placing all directories that need to be cloned and downloaded under the ~/ directory, because our scripts work according to this structure.

1) Clone HyFiSS from GitHub repository and build:

```
$ git clone https://github.com/ConvolutedDog/HyFiSS.git ~
```

```
$ cd ~/HyFiSS && make clean && make all -j
$ cd ~/HyFiSS/tracing-tool && make clean && make
$ cd ~/HyFiSS/sass-split && make clean && make
```

2) Clone Paper-Figures from GitHub repository:

```
$ git clone https://github.com/ConvolutedDog/Paper-Figures.git ~
$ mkdir ~/Paper-Figures/figs
```

3) Download Pre-Provided-Results.tar.gz from Zenodo repository, save it to the <Download>/ directory, move it into the ~/ directory, and unzip it:

```
$ wget -O <Download>/Pre-Provided-Results.tar.gz
  https://zenodo.org/records/13150677/files/Pre-Provided-Results
  .tar.gz?download=1
$ mv <Download>/Pre-Provided-Results.tar.gz ~/
$ cd ~/ && tar zxvf Pre-Provided-Results.tar.gz
$ rm ~/Pre-Provided-Results.tar.gz
```

4) Clone Results-Process-Scripts from GitHub repository:

```
$ git clone https://github.com/ConvolutedDog/Results-Process-
  Scripts.git ~
```

5) Clone Self-Simulated-Results from GitHub repository:

```
$ git clone https://github.com/ConvolutedDog/Self-Simulated-
  Results.git ~
```

6) Download simulator-apps.tar.gz from Zenodo repository, save it to the <Download>/ directory, move it into the ~/ directory, unzip it, and build:

```
$ wget -O <Download>/simulator-apps.tar.gz https://zenodo.org/
  records/13150677/files/simulator-apps.tar.gz?download=1
$ mv <Download>/simulator-apps.tar.gz ~/
$ cd ~/ && tar zxvf simulator-apps.tar.gz
$ rm ~/simulator-apps.tar.gz
$ cd ~/simulator-apps && ./cleanall.sh && ./buildall.sh
```

F. Experiment workflow

1) We have already provided a smoke-test script—named smoke-test.sh—in the ~/Self-Simulated-Results/Self-Simulated-GV100-Results/ directory, which simulates the *hotspot* application and can be used to verify whether HyFiSS can execute successfully. Users need to check the <GPU_ID> of the GV100 GPU, make it visible, and execute the smoke-test script:

```
$ nvidia-smi    # check the <GPU_ID> of the GV100 GPU
$ export CUDA_VISIBLE_DEVICES=<GPU_ID>
$ cd ~/Self-Simulated-Results/Self-Simulated-GV100-Results/
$ bash smoke-test.sh > smoke-test.log
```

   If the records in smoke-test.log show successful generation of reports, it indicates that the smoke-test has passed.

2) After the smoke test is successful, we will use configurations for the GV100 GPU and A100 GPU to simulate all applications in the ~/simulator-apps directory. Please note that real GV100 and A100 GPUs are required to extract the application's traces. This step may take a considerable amount of time, with each script running for 1 to 3 days, primarily depending on CPU performance:

```
$ nvidia-smi    # check the <GPU_ID> of the GV100 GPU
$ export CUDA_VISIBLE_DEVICES=<GPU_ID>
$ cd ~/Self-Simulated-Results/Self-Simulated-GV100-Results/
$ bash Self-Simulated-GV100-Results.sh > Self-Simulated-
  GV100-Results.log
$ nvidia-smi    # check the <GPU_ID> of the A100 GPU
$ export CUDA_VISIBLE_DEVICES=<GPU_ID>
$ cd ~/Self-Simulated-Results/Self-Simulated-A100-Results/
$ bash Self-Simulated-A100-Results.sh > Self-Simulated-A100-
  Results.log
```

3) Next, we will compare the simulation results of HyFiSS with our pre-provided results from Accel-Sim, PPT-GPU, and Nsight Compute, generating Excel files for the GV100 and A100 GPU configurations. Each Excel file will have a maximum of 7 sheets, and each sheet will contain 143 metrics for thousands of kernels. These files will be saved in the ~/Self-Simulated-Results/ directory, named compare_for_self_simulated_GV100_results.xlsx and compare_for_self_simulated_A100_results.xlsx, respectively:

```
$ cd ~/Self-Simulated-Results/Self-Simulated-GV100-Results/
$ ln -s ~/Pre-Provided-Results/Pre-Provided-GV100-Results/
  Accel-Sim-Results ./
$ ln -s ~/Pre-Provided-Results/Pre-Provided-GV100-Results/
  PPT-GPU-Results ./
$ ln -s ~/Pre-Provided-Results/Pre-Provided-GV100-Results/
  NsightCollection ./
$ cd ~/Self-Simulated-Results/Self-Simulated-A100-Results/
$ ln -s ~/Pre-Provided-Results/Pre-Provided-A100-Results/
  NsightCollection ./
$ cd ~/Results-Process-Scripts/
$ python3 read_reports_for_self_simulated_GV100_results.py
$ python3 read_reports_for_self_simulated_A100_results.py
```

   Note: If users utilize the provided docker image, executing the symbolic link step is unnecessary, as it has already been completed.

4) To reproduce the figures mentioned in the Artifact Appendix Abstract:

```
$ cd ~/Paper-Figures/
$ bash Paper-Figures-Self-Simulated.sh
```

   The reproduced figures, which are basically consistent with those inserted in our paper, will be located in the ~/Paper-Figures/figs/ directory.

G. Evaluation

We generate Figure 2a-Figure 2d using the absolute values of *Simulation Time (seconds)*, *Active Cycles*, *IPC*, and *Achieved Occupancy*. For other figures, we evaluate the error in predicting *Active Cycles* compared to *Nsight Compute* using the *Mean Absolute Percentage Error (MAPE)* for HyFiSS, Accel-Sim, and PPT-GPU. The *Mean Absolute Error (MAE)* is used to evaluate the error in predicting cache hit rates for the three simulators compared to *Nsight Compute*. We also use *Pearson's Correlation Coefficient (Corr.)* to evaluate the correlation between the predicted and measured metrics for the three simulators. Finally, We utilize normalized percentages to evaluate the *Distribution of Stall Types and Stall Events*, *Execution Time Distribution of Execution Units*, and *Executed Instructions Distribution of Execution Units* in Figure 13-Figure 14.

H. Expected results

All the expected results are illustrated in the figures, which are basically consistent with the results described in our paper.

I. Notes

1) The results of the bottleneck analysis are closely tied to the specific execution environment, particularly the runtime.
2) Utilizing the docker image may incur some loss in simulation speed compared to running on physical machines.

J. Methodology

Submission, reviewing and badging methodology:

- https://www.acm.org/publications/policies/artifact-review-badging
- http://cTuning.org/ae/submission-20201122.html
- http://cTuning.org/ae/reviewing-20201122.html

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